UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/620,470	07/15/2003	Lawrence T. Clark	MP1494	8637

26703 7590 11/16/2007

HARNESS, DICKEY & PIERCE P.L.C.
5445 CORPORATE DRIVE
SUITE 200
TROY, MI 48098

EXAMINER	
SUGENT, JAMES F	

ART UNIT	PAPER NUMBER
2116	

MAIL DATE	DELIVERY MODE
11/16/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/620,470	CLARK, LAWRENCE T.	
	Examiner	Art Unit	
	James F. Sugent	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 August 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,7,9-15,17-20 and 22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) *11-15,17-20 and 22* is/are allowed.

6)☐ Claim(s) *1-5,7,9 and 10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is sent in response to Applicant's Communication received August 29, 2007 for application number 10/620,470. The Office hereby acknowledges receipt of the following and placed of record in file: amended claims 1-22 (wherein claims 6, 8, 16 and 21 are canceled) presented for examination.

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 1-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Woods et al. (U.S. Patent No. 7,058,834 B2) (hereinafter referred to as Woods) in view of Stapleton et al. (U.S. Patent No. 6,574,577 B2) (hereinafter referred to as Stapleton).

As to claim 1, Woods discloses a method comprising: providing power to an integrated circuit (IC) (130) during an active mode (column 3, lines 12-23); moving an integrated circuit state of the IC into on-die storage (memory 270 within ISPRM 160) of the IC (column 4, lines 22-29 and column 4, lines 38-47 and column 7, lines 3-32); disabling power to on-die combinational circuitry (SPA) during a low power mode (sleep state) by disrupting power supplied from an external power supply regulator to the IC (column 4, lines 48-53 and column 2, line 49 thru column 3, line 2 and column 2, lines 1-10); and, supplying the power (via 204) from a power supply regulator (110) to the on-die combinational circuitry (130) (column 4, lines 55-60).

Woods fails to disclose the power being disabled externally; and, providing a power feedback signal from an internal portion of the IC to the power supply regulator.

Stapleton teaches a power control method that externally disables power (via 11) to an IC (12) (column 1, lines 40-57). Stapleton first teaches supplying power (via Vccp 15) from a power supply regulator (11) to the on-die combinational circuitry (12) (column 1, lines 41-48). Stapleton further teaches the power supply regulator (11) stops delivering power (Vccp) to the IC when another input voltage (Vtt) is de-asserted (column 2, lines 38-50). Stapleton continues to teach providing a power feedback signal (voltage ident signal 17) from an internal portion of the IC (12) to the power supply regulator (11) (as seen in Fig. 1; column 1, lines 49-67). Stapleton further teaches the additional benefit of ensuring a proper voltage is delivered thus preventing an improper, harmful voltage level to a chip (column 1, lines 15-26 and column 2, lines 49-57).

It would have been obvious to one of ordinary skill of the art having the teachings of Woods and Stapleton at the time the invention was made, to modify the method of Woods to include the ability of disabling power externally as taught by Stapleton. One of ordinary skill in the art would be motivated to make this combination of including the ability to externally disable power in view of the teachings of Stapleton, as doing so would give the added benefit of ensuring a proper voltage is delivered thus preventing an improper, harmful voltage level to a chip (as taught by Stapleton above).

As to claim 2, Woods in combination with Stapleton taught the method in claim 1, as shown above. Stapleton further teaches the method wherein disabling power further includes tri-stating an output of a power supply regulator that provides power to the on-die combinational circuitry (column 2, lines 38-50).

As to claim 3, Woods in combination with Stapleton taught the method in claim 1, as shown above. Stapleton further teaches the method wherein disabling power further includes gating an off-die clamp to disrupt power supplied from an external power supply regulator to the on-die combinational circuitry (column 4, lines 15-51).

As to claim 4, Woods in combination with Stapleton taught the method in claim 1, as shown above. Woods further teaches the method wherein disrupting the power further includes gating an on-die clamp (column 6, line 59 thru column 7, line 2).

As to claim 5, Woods in combination with Stapleton taught the method in claim 1, as shown above. Woods further teaches the method including reapplying power after the integrated circuit receives an interrupt (column 8, lines 11-30).

Claims 7 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stapleton (as cited above) in view of Heimbigner (U.S. Patent No. 4,363,978) (hereinafter referred to as Heimbigner).

As to claim 7, Stapleton discloses method comprising: forcing a high impedance state (tri-state) on an output of a power supply regulator (11) that is coupled to a power pin of an integrated circuit (12) (column 1, lines 40-57 and column 2, lines 38-50), wherein forcing the high impedance state (tri-state) includes de-asserting a drive pin (of 12) coupled to a gate of a power transistor (BJT 74 in Fig. 3) to force the high impedance state on the output of the power supply regulator (from 11 along Vccp 17) (column 2, lines 38-67 and column 3, lines 18-31 and column 4, line 32 thru column 5, line 3). [In summary, the power good circuit (16) de-asserts the POWER_GOOD signal that causes the voltage regulator (14) to set the Vccp output (to gate pin of 12) to a high impedance state (tri-state) (column 2, lines 42-46). The gate of a transistor (74)

within the power good circuit (16) that carries this out is coupled to the drive pin of the processor (via 14) (column 4, lines 32-51).]

Stapleton fails to teach the power transistor being a MOS power transistor.

Heimbigner teaches a method that uses a tri-state power driver to gate power to a load. The power driver (96) uses to CMOS transistors to deliver the load in three states of operation (column 1, line 65 thru column 2, line 23). Heimbigner has the additional feature of further reducing power delivered to a circuit (column 1, lines 31-36).

It would have been obvious to one of ordinary skill of the art having the teachings of Stapleton and Heimbigner at the time the invention was made, to modify method of Stapleton to include the power transistor being a MOS power transistor as taught by Heimbigner. One of ordinary skill in the art would be motivated to make this combination of the power transistor a MOS power transistor in view of the teachings of Heimbigner, as doing so would give the added benefit of further reducing power delivered to a circuit (as taught by Heimbigner above).

As to claim 10, Stapleton in combination with Heimbigner taught the method in claim 7, as shown above. Stapleton further teaches the method comprising: timing the de-assertion to avoid high voltages on a supply inductor coupled between the output of the power supply regulator and the power pin of the integrated circuit (Abstract and column 2, lines 1-10).

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Stapleton in view of Heimbigner as applied to claim 7 above, and further in view of Cruz (U.S. Patent No. 6,754,692 B2) (hereinafter referred to as Cruz).

As to claim 9, Cruz teaches a power distribution circuit (100) that includes a diode (140) which keeps current from flowing into a circuit's power supply system which is inclusive of a

MOS transistor (170) (column 2, lines 24-60 and column 6, lines 14-29). Cruz further teaches the additional benefit of electronically isolating power buses from power domains (column 1, lines 33-53 and column 2, lines 49-60).

It would have been obvious to one of ordinary skill of the art having the teachings of Stapleton and Cruz at the time the invention was made, to modify power supply regulator of Stapleton to include a diode to a source MOS power transistor as taught by Cruz. One of ordinary skill in the art would be motivated to make this combination of including a diode in the power supply regulator in view of the teachings of Cruz, as doing so would give the added benefit of electronically isolating power buses from power domains (as taught by Cruz above).

Allowable Subject Matter

Claims 11-15, 17-20 and 22 are allowed.

The following is a statement of reasons for the indication of allowable subject matter: presented in previous office action.

Response to Arguments

Applicant's arguments filed August 29, 2007 with respect to claim 1 have been considered but are moot in view of the new ground(s) of rejection.

In re claim 7, Applicant's arguments filed August 29, 2007 have been fully considered but they are not persuasive. Applicant argues that Stapleton fails to disclose "de-asserting a drive pin coupled to a gate of a MOS power transistor to force the high impedance state" (REMARKS, page 8, lines 17-19). The Examiner disagrees and stands by the rejection presented hereinabove

under 35 USC § 103(a). Stapleton discloses power being delivered (from 11 via Vccp 17) to a drive pin (of 12 of Fig. 1 which is a processor and inherently necessitates a drive pin) wherein the power is asserted and de-asserted to the processor (12) (column 1, lines 41-67 and column 2, lines 38-50). The de-assertion is carried out by a voltage regulator (14 found within the power system 11) such that the output of the voltage regulator (14) is tri-stated (high impedance state) and not provide power (Vccp) to the processor (12) (column 2, lines 38-50). This is carried out by a power good circuit (16 found within power system 11) that comprises a transistor (BJT 74 within 16 of Fig. 3) such that a gate of the transistor (74) is coupled to the drive pin (via 14) of the processor (12) (column 4, line 32 thru column 5, line3). In summary, the power good circuit (16) de-asserts the POWER_GOOD signal that causes the voltage regulator (14) to set the Vccp output (to gate pin of 12) to a high impedance state (tri-state) (column 2, lines 42-46). The gate of a transistor (74) within the power good circuit (16) that carries this out is coupled to the drive pin of the processor (via 14) (column 4, lines 32-51). The limitation that the power transistor is a MOS power transistor is relied upon by the Heimbigner reference as also shown hereinabove. Therefore, claim 7 stands rejected under 35 USC § 103(a) as being unpatentable over Stapleton in view of Heimbigner.

Examiner has cited particular columns and line numbers in the references as applied to the claims above for the convenience of the Applicant. Although the specified citations are representative of the teachings of the art and are applied to the specific limitations within the individual claim, other passages and figures may apply as well. In preparing responses, it is respectfully requested that the Applicant fully consider the references in entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by

the prior art or disclosed by the Examiner. Also, any prior art made of record and not relied upon is also considered pertinent to Applicant's disclosure.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to James Sugent whose telephone number is (571) 272-5726. The Examiner can normally be reached on 8AM - 4PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Rehana Perveen can be reached on (571) 272-3676. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at (866) 217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call (800) 786-9199 (IN USA OR CANADA) or (571) 272-1000.

James F. Sugent
Patent Examiner, Art Unit 2116
November 7, 2007

A. ELAMIN
PRIMARY EXAMINER